TECHNICAL BULLETIN

UNIVAC | CUSTOMER SERVICES DIVISION

CONTENTS

SECTION 5

1219 (CP-848) COMPUTER

1219 AND 1219A MAIN MEMORY ADJUSTMENT PROCEDURE

CAUTION:

BEFORE MAKING ANY ADJUSTMENTS TO THE MEMORY, MAKE SURE YOUR PROBLEM LIES IN POOR ALIGNMENT. IT IS ALSO A GOOD PRACTICE TO RECORD THE MEMORY CURRENTS AND VOLTAGES BEFORE MAKING ANY ADJUSTMENTS IN CASE POOR ALIGNMENT IS NOT YOUR PROBLEM.

INITIAL CURRENT SETTINGS:

Inhibit Current - 270 ma.
Write Current - 250 ma.
Read Current - 240 ma.

SCOPE SETTINGS:

Make sure the scope is calibrated. Use a 10X probe with attached ground lead.

V/CM: .1
Time/CM: 1 USEC/CM
Trigger: AC fast, ext.

COMPUTER SETTINGS:

Master clear
Run Mode
Function Repeat
Set F - register to 44_8
Depress start switch

SUGGESTED PROCEDURE:

STEP 1: Check the +10 volts (inhibit) for the maximum ripple voltage of .1 volts as indicated in Table 1.

STEP 2: Set up the memory currents as indicated in Table 2.

STEP 3: SENSE AMP BIAS SETTING
Use a DC voltmenter to measure the -7 volts and extend the 7002861 card if adjustment is needed. Use Table 1 for proper test points and card locations.

STEP 4: After changing any potentiometers, recheck all readings before proceeding.

STEP 5: Replace the sense amp bias card if removed. Load and cycle the memory maintenance test (DS4790-3). Skips 2 and 4 should be set as well as stop Ø.

STEP 6: If errors occurs, proceed to STEP 7. If no error occurs, proceed to STEP 11.

STEP 7: Determine whether bits are being dropped or picked up.

STEP 8: If bits are being dropped, monitor the +10 volt supply at the test point specified in Table 1 and raise it slowly until errors do not occur. It should not be necessary to raise the supply more than 2 volts.

STEP 9: If bits are being picked up, monitor the +10 volt supply and lower it slowly until errors do not occur. It should not be necessary to lower the supply more than 2 volts.

STEP 10: If one or more particular bits continue to fail, check the associated sense amp or inhibit driver.

STEP 11: CENTER POINT OF THE +10 VOLT SUPPLY
Cycle the memory maintenance test. Monitor the +10 volt supply at the test point specified in Table 1 and raise the +10 volts until error occurs, as evidenced by stop Ø indication. Record the voltage. Lower the +10 volt supply until errors again occur, noting the voltage at the low end. Center the potentiometer at the mid-point of its operating range.

STEP 12: Do the same for the Sense amp bias, the -7 volt supply as specified in Table 1, until it, too, is set at its mid-point.

STEP 13: After adjustments have been made, continue to cycle the memory test on all margins for at least one hour for added confidence.

Table 1. Voltage Settings

DRAWER	VOLTAGE	TEST POINT	GROUND	ADJUST
A3				
(Addresses 000000-037777)	-7.0V	E27	A27	6H11G
	+10V (Inhibit)	F27	A27	A4R24
Chassis 6				
A3				
(Addresses 040000-077777)	-7.0V	E17	A17	5J11G
	+10V (Inhibit)	F17	A17	A4R14
Chassis 5				
A9				
(Addresses 100000-137777)	-7.0V	E27	A27	12J11G
	+10V (Inhibit)	F27	A27	A4R44
Chassis 12				
A9				
(Addresses 140000-177777)	-7.0V	E17	A17	11J11G
	+10V (Inhibit)	F17	A17	A4R54
Chassis 11				

Table 2. Memory Current Settings

DRAWER	CURRENT	SCOPE PROBE	GROUND LEAD	CURRENT	ADJUST	SCOPE SYNC
A3	Inhibit	A22	A23	270 ma	A4R24(+10V)	
(Addresses 000000-	X-Read	A20	A21	240 ma	A4R22(XR)	C26
037777)	X-Write	B20	B21	250 ma	A4R23(XW)	
Chassis 6	Y-Read	C20	C21	240 ma	A4R20(YR)	
	Y-Write	D20	D21	250 ma	A4R21(YW)	
A3	Inhibit	A12	A13	270 ma	A4R34(+10V)	
(Addresses 040000-	X-Read	A10	A11	240 ma	A4R32(XR)	
077777)	X-Write	B10	B11	250 ma	A4R33(XW)	C16
Chassis 5	Y-Read	C10	C11	240 ma	A4R30(YR)	
	Y-Write	D10	D11	250 ma	A4R31(YW)	
A9	Inhibit	A22	A23	270 ma	A4R44(+10V)	
(Addresses 100000-	X-Read	A20	A21	240 ma	A4R42(XR)	
137777)	X-Write	B20	B21	250 ma	A4R43(XW)	C46
Chassis 12	Y-Read	C20	C21	240 ma	A4R40(YR)	
	Y-Write	D20	D21	250 ma	A4R41(YW)	
A9	Inhibit	A12	A13	270 ma	A4R54(+10V)	
(Addresses 140000-	X-Read	A10	A11	240 ma	A4R52(XR)	C56
177777)	X-Write	B10	B11	250 ma	A4R53(XW)	
Chassis 11	Y-Read	C10	C11	240 ma	A4R50(YR)	
	Y-Write	D10	D11	250 ma	A4R51(YW)	

1219 and 1219A VOLTAGE FAULT ADJUSTMENT

There is a voltage fault detection circuit which senses both catastrophic voltage failures and voltage decreases of greater than 10% of the minimum input voltage requirement. This circuit enables the computer's memory to retain data during a power loss or line transient.

At 100 volts the voltage fault and abnormal condition indicators will light and the alarm will sound. If battle short is on, the computer will continue running, if not, the memory cycle that is in process is allowed to finish, the program run indicator is extinguished, and then the computer is master cleared.

SUGGESTED PROCEDURE:

STEP 1. Remove power from the equipment.

STEP 2. Connect a variac to the 400 cycle input line. The MG controller may be used in place of a variac if all equipment, other than the computer, on the MG system are powered off.

STEP 3. Open memory chassis A3 (and A9 if memory greater than 32K) and remove the 2880 and 3270 cards in locations J12A and J11A respectively, in each side of the chassis.

STEP 4. Insert a card extender in jack location J12A of chassis A3A1.

STEP 5. Close and tighten down all memory chassis.

STEP 6. Insert one of the 2880 cards into the card extender and connect the scope probe to test point A8TB1-G16. (12G81 fig. 9-122).

STEP 7. Bring up power and adjust the variac to 100 volts.

STEP 8. Adjust one of the potentiometers on the 2880 card until the signal on the scope has just gone negative and then back it off so that it is just positive again. Adjust the second potentiometer in the same manner.

STEP 9. Adjust the variac to about 110 volts, then master clear the computer.

STEP 10. Reduce the variac until the computer voltage fault indicator lights. This is the voltage fault voltage.

STEP 11. Re-adjust the variac to 100 volts.

STEP 12. De-Energize the equipment and replace the 2880 card just adjusted with one of the other 2880 cards. Energize the equipment and repeat step 8 thru 11 for the other 2880 cards.

STEP 13. When all 2880 cards have been adjusted de-energize the equipment and place the card extender in J11A of the same chassis.

STEP 14. Insert one of the 3720 cards in the card extender.

STEP 15. Energize the equipment.

STEP 16. Adjust the potentiometer on the 3720 card until the signal on the scope has just gone negative and back it off so that it just goes positive again.

STEP 17. Repeat steps 9 thru 11 using the 3720 card.

STEP 18. De-energize the equipment and replace the 3720 card just adjusted with one of the other 3720 cards. Energize the equipment and repeat steps 16, 9, 10, and 11 for the other 3720 cards.

STEP 19. De-energize the equipment.

STEP 20. Open memory chassis and replace the 2880 cards in location J12A and the 3720 cards in location J11A of each side of the memory chassis. Close the chassis.

STEP 21. Energize the computer and repeat steps 9 and 10 to determine the voltage fault voltage. If not 100 volts, re-adjust the cards and compensate for any variance due to the use of the card extender.

STEP 22. Remove the variac, if used, and reset the 400 cycle power source to the 115 volt operating point.

The memory protection circuits can be checked by running any maintenance program and dropping input power. When the computer is turned on and the program is restarted it should run without any instruction loss. Note that some tests relocate themselves in memory and must be restarted at their relocated starting address.

1219 CONTROL MEMORY ADJUSTMENT PROCEDURE

The performance of the 1219, 1219A, 1219B control memory can be improved, especially under conditions of extreme temperature variation, by narrowing the strobe pulse width from the factory adjusted 140 nsec. to 80 nsec. ± 5 nsec. This change can be accomplished by qualified personnel in the field if the proper procedures are used. Strobe pulse timing, as well as strobe pulse width, is critical and should be observed as specified in the following procedure before any adjustments are attempted.

TEST EQUIPMENT REQUIRED

Tektronic 585A Scope
Tektronix current Probe Type P6016 with Tektronix Current Probe Termination
Weston Model 931 Precision DC Voltmeter
Test leads for the above meter
Scope Probes and External Sync. Lead
Blade Screwdriver ¼ inch
Blade Screwdriver 1/16 inch
15 pin P.C. Card extender

INITIAL SETTINGS

+ Voltage regulated supply

Measure the DC voltage at TB2-C33 on chassis 8 with the precision meter. Using the pot marked + V, located on the front panel if the computer S/N is under 10, and on the chassis next to the test points if S/N 10 and above, adjust the voltage for +17 VDC.

- Voltage Regulated Supply

Measure the voltage at TB2-B33 on chassis 8 with the precision meter. Using the pot marked -V, located on the front panel if the S/N is under 10, and on the chassis next to the test points if S/N 10 and above, adjust this voltage for -16 VDC.

Read/Write Currents

Adjust the read/write current pots with the ¼ inch screwdriver to the mechanical center of their rotation between stops.

Sense Bias Voltage Supply

Open the A4 drawer and place the P.C. Card at 8J20D in the 15 pin card extender. Close the drawer and adjust the pot on the P.C. Card in the following manner. Measure the voltage at TB2-A33. Adjust the pot on the card for -7 VDC. Select Function Repeat, Disconnect Advance P, Set the F Register to 44, Set AL Register to all "ones", Set Run Mode, and push the Start Step switch. Using the Scope, Ext. Trigger at TB2-C10 on chassis 8, compare the Strobe Pulse (TB1-G25 on chassis 8) with the Sense Read-out for Bit 0 (TB2-A31 on chassis 8). Observe that the Strobe Pulse is wider than the sense read-out and completely "brackets" the sense read-out for bit 0. If the timing has not been changed since the computer left the factory, the Strobe Pulse width

should be 140 nsec. and all of the delay line taps should be as specified on Fig. 9-122 Rev. A of the Functional Schematics. Strobe initiation (input to 30EF04) and Strobe Termination (input to 30EF05) should be adjusted if the Strobe Pulse is over 80 nsec. or if the timing is incorrect. After the necessary adjustment of the strobe pulse, final adjustments should be made as follows. Cycle the computer through the lower 100$_8$ addresses of control memory by grounding bit 6 of the P Register (test point TB1-A31 on chassis 4) and releasing Disc. Adv. P (computer set-up as above with the exception of Disc. Adv. P.). Look at all the Sense outputs (Fig. 9-131) and make sure that they are 80 nsec. $\pm$ 5 nsec. wide and that the control memory strobe completely "brackets" the read-outs with 5 to 10 nsec. overlap. The sense bias voltage may have to be re-set to widen or narrow the read-out for the weakest bit.

With the above adjustments completed, the computer should operate well enough to load and run FACT control memory test. A failure in loading would indicate a failing part in memory or some other related cause not associated with improper adjustments. If some cards were changed in the control memory timing circuitry, it is possible that further timing adjustments may be necessary.

FINE ADJUSTMENTS

After the control memory test is cycling properly, the control memory regulated voltages should be adjusted to provide optimum performance in the following manner:

+ Voltage Regulated Supply

Monitor the voltage at TB2-C33 on chassis 8 with the precision DC Volt meter and raise the voltage until the control memory test fails and record this voltage. Restart the computer and lower the voltage until the test fails again. Record this voltage. Set the +V midway between the points of failure.

- Voltage Regulated Supply

Monitor the voltage at TB2-B33 on chassis 8 with the precision DC volt meter while running the control memory test and raise the -V until the test fails. Record this voltage, restart the computer and lower the voltage until it fails again. Record this voltage and set the -V midway between the points of failure. Repeat the +V and -V adjustments at least twice to achieve optimum performance of the control memory.

Read/Write Currents

These pots should be variable from minimum to maximum without causing an error in the test, if the voltage adjustments are properly made. However, an error occurring at the extreme ends of these pots does not necessarily mean that the control memory is bad. Some computers just will not have as good margins as others. Failures of the same bits would indicate marginal sense amplifiers or digit driver cards. Sense bias voltage may have to be touched up while observing "worst-case" sense outputs to ensure proper operation.

The read/write current pots should be returned to approximately their midpoint range. By reading continuously out of a control memory address measure the current pulses with a current probe. The read current should be between 400-500 ma. and the write current between 300-400 ma.

If the S/N is under 10, the two wires M1 and M2 going into Jack 41 on the control memory allows you to check both currents at the same time. Wire M1 is for checking the read current and the upper pot is the adjustment. Wire M2 is for checking the write current and the lower pot is the adjustment.

On S/N 10 and above, the two jumper wires between two studs located by the read/write pots allows you to check the currents without removing the chassis. The upper wire, TP-1 is for checking the read current and the upper pot is the adjustment. The lower wire, TP-2 is for checking the write current and the lower pot is the adjustment.

While observing the memory currents if you vary the pots from one limit to the other the read current should vary approximately 150 ma. and the write current approximately 100 ma. If the currents fail to vary while changing the pots, the indication would be a failing part in the associated circuitry. It is also possible that the control memory timing is misadjusted, however, if it hasn't been touched it should be correct.

If the control memory is operating satisfactorily, the following adjustments can be varied according to the chart below while cylcing the control memory test without an error.

	FROM	TO
+VDC	+12 VDC	+19 VDC
-VDC	-10 VDC	-20 VDC

1219B MAIN MEMORY ADJUSTMENT PROCEDURE

CAUTION: BEFORE MAKING ANY ADJUSTMENTS TO ANY MEMORY CHASSIS, MAKE SURE YOUR PROBLEM LIES IN POOR ALIGNMENT. IT IS ALSO A GOOD PRACTICE TO RECORD THE MEMORY CURRENTS AND VOLTAGES BEFORE MAKING ANY ADJUSTMENTS IN CASE POOR ALIGNMENT IS NOT YOUR PROBLEM.

NOMINAL CURRENT SETTINGS:

X Read/Write Current---820 ma. P-P
Y Read/Write Current---820 ma. P-P
Inhibit Current---800 ma.
Sense Bias ---------- -6 volts

COMPUTER SETTINGS:

Master Clear
Function Repeat
Disconnect ADV P
Set F - Register to 44g
Set P - Register to 01000g if checking BANK 0
Set P - Register to 40000g if checking BANK 1
Depress start switch

NOTE: DO NOT ATTEMPT TO RUN THE COMPUTER WITH THE MEMORY CHASSIS EXTENDED FOR ANY LENGTH OF TIME WITHOUT SUPPLEMENTARY COOLING SUCH AS A FAN.

SUGGESTED PROCEDURE:

STEP 1. To check the currents place the current probe as follows for BANK 0.

X Read/Write	A1 **F23**	Located behind stack 0
Y Read/Write	A1 **W2**	Located behind stack 0
Inhibit	A1 **A4** and **B4**	Black and white twisted pair located behind stack 0

STEP 2. Set currents and voltage as follows for BANK 0.

X Read/Write	820 ma. P-P	Adjust gJ30B (Top pot)
Y Read/Write	820 ma. P-P	Adjust gJ30B (Second pot down)
Inhibit	800 ma.	Adjust gJ30B (Third pot down)
Sense Bias	-6 volts at TP-5gJ30B	Adjust gJ30B (Bottom pot)

STEP 3. To check the currents place the current probe as follows for BANK 1 (be sure P- Register equals 40000).

X Read/Write	D1 **F23**	Located behind stack 4
Y Read/Write	D1 **W2**	Located behind stack 4
Inhibit	D1 **A4** and **B4**	Black and red twisted pair located behind stack 4

STEP 4. Set currents and voltage for BANK 1 the same as BANK 0 in STEP 2 except use card location gJ30D.

STEP 5. Load the integrated memory test and cycle on normal basis.

NOTE: If any errors occur at this time isolate and correct the problem. Any errors here are assumed to be non-current adjustment errors.

STEP 6. Reduce the sense bias referenced to in STEP 2 in .5 volt increments until the test fails, note this voltage.

NOTE: Be sure to let the test cycle completely at each increment. The test may have to be reloaded after failing since the program may be partially destroyed.

STEP 7. Return the sense bias to 6 volts and cycle the test.

STEP 8. Increase the sense bias in .5 volt increments until the test fails, note this voltage. The sense bias should be able to be varied between 3 and 9 volts without any errors. If errors are encountered, note if it is the same bit every time, this indicates a possible bad card. If the failing bits vary, try increasing the read/write currents a turn or two if the errors occur on lower margins. Decrease the currents if the upper margin has errors.

1219B VOLTAGE FAULT ADJUSTMENT

There are two detection circuits which must be adjusted for 104 and 101 VAC input logic voltage respectively. These circuits enable the computer's memory to retain data during a power loss or line transient.

At 104 volts the voltage fault and abnormal condition indicators will light and the alarm will sound. If battle short is on, the computer will continue running, if not, the memory cycle that is in process is allowed to finish and the program run indicator is then extinguished.

At 101 volts the detection circuit in each 32K section of the memory drawer will disable the inhibit drivers regardless of the position of the battle short switch. After a power failure condition, the computer must be turned off and power reapplied to enable the inhibit drivers.

SUGGESTED PROCEDURE:

Setting the 104 volt circuit.

STEP 1. Remove power from the equipment.

STEP 2. Connect a variac to the 400 cycle input line. The MG controller may be used in place of the variac if all equipment other than the computer on the MG system are powered off.

STEP 3. Open chassis A4A1 and remove the 2880 and 3720 cards at locations J34E and J34F respectively.

STEP 4. Insert card extender in J34E and close the chassis.

STEP 5. Put the 2880 card in the extender and connect a scope probe to test point A7TB2-D25. (12G81 on Fig. 9-134).

STEP 6. Bring up power and adjust the variac to 104 volts.

STEP 7. Adjust one of the potentiometers on the 2880 card until the signal on the scope has just gone negative and then back it off so that it is just positive again. Adjust the second potentiometer in the same manner.

STEP 8. Adjust the variac to about 110 volts, then master clear the computer.

STEP 9. Reduce the variac until the computer voltage fault indicator lights. This is the voltage fault voltage.

STEP 10. Re-adjust the variac to 104 volts.

STEP 11. De-energize the equipment and remove the 2880 card from the card extender.

STEP 12. Move the card extender to J34F of the same chassis and insert the 3720 card.

STEP 13. Energize the equipment.

STEP 14. Adjust the potentiometer on the 3720 card until the signal on the scope has just gone negative and back it off so that it just goes positive again.

STEP 15. Repeat steps 8 and 9.

STEP 16. De-energize the equipment.

STEP 17. Remove the card extender and re-insert the 2880 and 3720 cards in 34E and 34F respectively.

STEP 18. Energize the computer and repeat steps 8 and 9 to determine the voltage fault voltage. If not 104 volts, re-adjust the cards and compensate for any variance due to the use of the card extender.

Setting the 101 volt circuit.

STEP 1. Connect a scope probe to test point TP1 on the 0340 card at J11C of chassis A3A2 (the first 32K of memory). (00VS00 on fig. 9-145)

STEP 2. Adjust the variac to 101 volts.

STEP 3. Adjust the potentiometer on the 0340 card at J11C of chassis A3A2 until the signal on the scope has just gone negative and then back it off so that it is just positive again.

STEP 4. Repeat steps 1 thru 3 for chassis A3A1 if the computer has more then 32K of memory.

STEP 5. Remove the variac, if used, reset the 400 cycle input line to the 115 volt operating point.

The memory protection circuits can be checked by running any maintenance program and dropping input power. When the computer is turned on and the program is restarted it should run without any instruction loss. Note that some tests relocate themselves in memory and must be restarted at their relocated starting address.

1219B MISCELLANEOUS NOTES

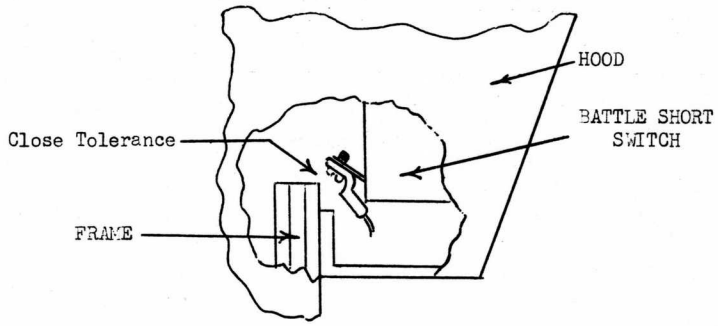
POSSIBLE SHORTING PROBLEM

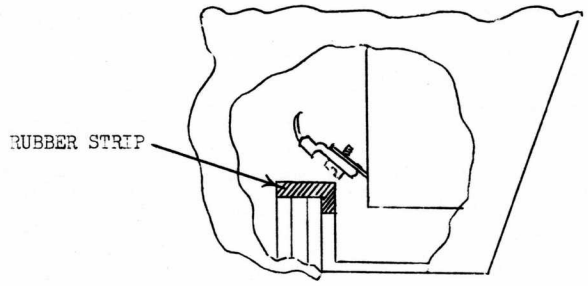
A possible shorting problem can exist in the 1219B computer. During assembly and wiring of the "BATTLE SHORT" switch, some 1219B computers could have a very close tolerance between the terminal lugs on the "BATTLE SHORT" switch and the frame. All 1219B computers should be checked for this condition. If a close tolerance is found, which could cause a short if the computer is subjected to heavy vibration, use one or both of the two recommended methods to cure the problem.

CAUTION: There is power at the "BATTLE SHORT" switch even though the computer power is turned off. Turn Motor Generator off before removing the switch panel (Hood).

1. Loosen terminal contacts on rear of "BATTLE SHORT" switch, loosen lacing, and turn lugs so they are pointing to the rear. This will allow more clearance between terminal lugs and frame.

2. There is a small kit, available from UNIVAC, which consists of an "L" shaped strip of rubber and adhesive which can be mounted on the frame. This will prevent the lugs from contacting the metal frame.





UNIVAC EQUIPMENT MANUALS

HARDWARE

PRODUCT	NAME	S/N	PX NO.
1219	1219A Computer, Volume I	10,11, & 13	3316-1-3
	1219A Computer, Volume II	10,11, & 13	3316-2-3
	1219 Diagnostics, Volume I	1-11 & 13	3520-1-2
	1219 Diagnostics, Volume II	1-11 & 13	3520-2-2
	1219 Maintenance Study Guide	1-11 & 13	3814-0-1
	1219 Programming Study Guide	1-11 & 13	3943-0-2
	1219 Programming Study Guide		3943-0-3
	1219B Computer, Volume 1		4682-1-2
	1219B Computer, Volume II		3682-2-2
	1219B Maintenance Study Guide		5057-0-1
	1219B Diagnostics, Volume I		4637-1-1
	1219B Diagnostics, Volume II		4637-2-1
	1219B Diagnostics, Volume III		4637-3-1

SOFTWARE

PRODUCT	NAME	S/N	PX NO.
1219	1219, Programmers Reference Manual		3288
	1219, Programmers Study Guide		3943-0-2
	The ULTRA/18-1 Assembler User's Manual and Programmers Reference Manual		4901
	1219B Programmers Reference Manual		4939
	SYCOL for 1219		4171
	FORTRAN for 1219		4165

FIELD CHANGE ORDERS

(This section covers Field Change Orders through July 1980)

The purpose of this section is to provide information on most Field Change Orders that are applicable to this piece of equipment. It contains the PDS number, the FCO numbers, a general statement of their purpose, and the serial numbers of the units affected by the FCO's.

NOTE: Some FCO's were generated for special projects even though the FCO could be applied to units not included in the serial effectivity. In such cases where the customer may want to install the FCO in their units, the FCO kit may be purchased through their UNIVAC contracts representative. Some tables have been removed from this section to make room for new equipments. If you have any questions as to whether or not an FCO could apply to your unit, contact the following:

Sperry Univac
Defense Systems Division
Univac Park, P. O. Box 3525
St. Paul, MN 55165

Attn: MS S1B07
Oscar Wolske

or call (612) 647-4517

TABLE 1-6. FIELD CHANGE ORDERS FOR
1219 Computer (CP-848(V)/UYK)

PDS #1219

FCO	DESCRIPTION	S/N AFFECTED
MPL-130	Replace substitute parts used in manufacturing.	1,2
MPL-147	Avoid a possibility of processing an interrupt during an Interrupt Lockout period.	1,2
MPL-153	Change method of mounting card jacks for proper grounding	1-5
MPL-156	4030 Cards which are being replaced are too powerful and provide signal transients.	1,2
MPL-173	Replace indicator drivers if remote console is used.	1,2
MPL-181	Replace experimental cards with Product Line P.C. Cards	0,1
MPL-187	Correct logic error to prevent processing interrupts during B1 or B2 Seq.	1-5
MPL-192	Provide a test point for the inverter fed by the Low Speed Oscillator.	1-3,5
MPL-198	Master clear of F/F OXDT10.	1-6
MPL-236 Rev. A	Allow a shift instruction to be completed in the specified time.	1,2,4-6
MPL-238	Prevent RUN F/F from being set when powering up	1,2,4,5
MPL-239	Provide a master clear for the SØ Register and the BOOTSTRAP F/F.	1,2,4-6
MPL-240	Install bleeder resistors across capacitors in power supply	1-6
MPL-241	Logic error: 5014 instruction cleared INPUT ACTIVE F.F.	1-6
MPL-252	Eliminates interference between I/O sequencing or CMD and Control Memory Timing.	1-5
MPL-264	Exchange 4 male with 4 female connectors, and vice versa, on memory chassis.	1-5
MPL-284	Corrects function of EF/OD Ack. at maximum I/O rates	0-8
MPL-296	Correct logic error for 5036 instruction	0-7
MPL-319	Change lettering on input channel I/O jacks	5
MPL-336	Eliminate noise spikes by extra long clock lines.	10

TABLE 1-6. FIELD CHANGE ORDERS FOR
1219 Computer (CP-848(V)/UYK)

PDS #1219

FCO	DESCRIPTION	S/N AFFECTED
MPL-340	Superceded by MPL-341	
MPL-341 Rev. A	Add capacitor (C-3) to hood assembly (Supercedes MPL-340)	0-13
MPL-352	Corrects a miss wire for grounding on term 01D02	0-13
MPL-353	Removes an unused wire in the I/O command circuitry	0-13
MPL-373	Reverse fuse in hood assembly for easy access	0-13
MPL-374	Add capacitor (C-3) to hood assembly	10-13
MPL-383	Corrects timing interference between EXT. SYNC. REQ. and INTERRUPT sequence	0-13
MPL-406	Prevents I/O interrupts from being processed during LOAD Mode.	0-17
MPL-429	Corrects a timing problem between clearing the I/O Translator and the I/O Function Code Translator when I/O instruction is executed in control memory.	0-13
MPL-441	Shorten time constant for Resume Fault Int. (Per customer request thru contracts only)	10,13
MPL-468	Memory expansion from 32K to 64K by adding memory chassis only (Per customer request thru contracts only)	2
MPL-469	Memory expansion from 16K to 32K (Per customer request thru Contracts only)	6
MPL-479 Rev. A	Corrects timing problem between command signals and the setting and clearing of the P register.	0-13
MPL-536	Correct possible intermittent failure to set RESUME FF.	0-17
MPL-537	Correct intermittent I/O termination timing problem.	12,14-17
MPL-544 Rev. B	Inhibits INT between 5026 or 5027 and next instruction. Prevents hangup on RESUME time-out or 5026-5027.	0-46
MPL-593	Adds twisted pair to clock harness wiring and 220 ohm resistors to A1A2 and A8A2 to eliminate noise	14-22
MPL-594 Rev. B	Inhibits main memory from being altered while using bootstrap.	14-45
MPL-595	Replace 7500670 P.C. Card with 7500671.	12,14-45

TABLE 1-6. FIELD CHANGE ORDERS FOR
1219 Computer (CP-848(V)/UYK)

PDS #1219

FCO	DESCRIPTION	S/N AFFECTED
MPL-597	Replace 7500430 and 7500780 P.C. Cards with 7500431 and 7500781. Also remove 3 transistors.	12,14-45
MPL-601	Adds 1218 NTDS Compatible Mode, Bootstrap Mode Switch	12
MPL-610	Adds ground stud to memory drawer and decreases the +3 VDC ripple.	14-45
MPL-611	Correct dual channel 1218 Mode operation for proper buffer termination.	12,14-46
MPL-638	Install resistor in series with indicators to reduce load on indicator drivers.	14-17,20,21
MPL-669	Corrects a wiring error	49-53
MPL-783	Memory expansion from 32K to 48K (per customer request thru contracts only)	10,13
MPL-802	Rework 7500651 P.C. Cards.	76-81,112, 113
MPL-823	Correct a marginal condition apparent only on a divide by -(NEG) Y.	14-120
MPL-919	Add resistor A4R1, A4R2, and change value of A2R48 to improve Control Mem margins S/N AFFECTED: 16,20-26,29-40,42-48,50-54,58,59,62, 74,75,106,107,114-117,120,122,123,130-132	14-132
MPL-1001	Correct critical timing problem during intercomputer. S/N AFFECTED: 1-11,13,16,20-26,29-35,37-40,42-48, 50-54,58,59,62,74,75,106,107,114,117,122,130,131, 141,142,155-157,161-164	
MPL-1165	Allow overflow to be set when the RTC is on and F=20,23 instructions are executed.	0-211
MPL-1285	Correct the setting of bits in "F" register when executing format II instructions. S/N AFFECTED: 1-13,16,20-26,29-40,42-44,46-48, 50-54,58,59,62,74,75,106,107,114-117,122,123,130,131, 141,142,152,153,155-157,161,175,208,214,224. S/N 120,123,132,and 139 available for purchase.	
MPL-1707	Memory expansion from 32K to 64K.	153

UNIVAC 1219 (CP-848) COMPUTER BOOTSTRAP ASSEMBLIES

FINAL ASSEMBLY	PROGRAM ASSEMBLY	DESCRIPTION
7024774-02	7025706-00	1232-1532 Paper Tape, Ch. 0, 6 Level, Octal
7024774-05	7033107-00	1240 Mag Tape, Ch. 7, Mod. 6, (Dual Channel), 556 FPI, Bi-Octal, Odd Parity
7024774-06	7033157-00	1004 Card Processor/with Standard Test Board (4010507-00), Single Channel, Ch. 11
7024774-09	7046678-00	1240-1540-1541 Mag Tape, Ch. 7, Mod. 6 (Dual Channel), 556 FPI, Octal, Odd Parity
7024774-10	7046680-00	1240-1540 Mag Tape, Ch. 13, Mod. 3, 556 FPI, Octal, Odd Parity
7024774-11	7046684-00	1232-1532 Paper Tape, Ch. 7, 6 Level, Octal
7024774-15	7046691-00	1232-1532 Paper Tape, Ch. 13
7024774-16	7116226	1240-1540 Mag Tape, Ch. 1, Mod. 3, 200 FPI, Octal, Odd Parity
7024774-17	7116231	1240-1540-1541 Mag Tape, Ch. 7, Mod. 3, Single Channel, 556 FPI, Octal, Odd Parity
7024774-18	7116235	1240-1540 Mag tape, Ch. 7, Mod 3, Single Channel, 556 FPI, Bioctal, odd parity
7024774-19	7116236	1240-1540, Mag Tape, Ch. 3, Mod 3, Single Channel, 556 FPI, Bioctal, odd parity

1219 BOOTSTRAPS (PAPER TAPE)

ASSEMBLY	DESCRIPTION	ASSEMBLY	CHANNEL	DESCRIPTION
7025706-00	1232, 1532, Ch. 0, 6 Level, Octal, Ref. File U-8164	7046691-00	13	1232, 1532, Level 6, Octal, Ref. File U-8165

Address	Instruction	Address	Instruction
500	50-3400	500	50-3400
501	50-7310	501	50-7310
502	50-7201	502	36-0366
503	50-1300	503	12-0537
504	00-0534	504	45-0011
505	00-0534	505	73-0504
506	36-0000	506	50-1300 +k
507	42-0003	507	00-0537
510	70-0002	510	00-0537
511	44-0004	511	36-0000
512	70-0000	512	42-0123
513	50-1100	513	70-0002
514	00-0002	514	44-0124
515	00-0002	515	70-0000
516	50-2100	516	50-1100 +k
517	34-0516	517	00-0122
520	50-4606	520	00-0122
521	51-0002	521	50-2100 +k
522	63-0525	522	34-0521
523	10-0003	523	50-4606
524	60-0513	524	51-0122
525	57-0004	525	63-0530
526	34-0513	526	10-0123
527	45-0536	527	60-0516
530	56-0533	530	57-0124
531	34-0507	531	34-0516
532	34-0540	532	45-0536
533	00-0147	533	56-0536
534	00-0151	534	34-0512
535	00-0000	535	34-0540
536	00-0000	536	00-0147
537	00-0000	537	50-3151

1219 BOOTSTRAPS

(PAPER TAPE)		(MAG TAPE)	
ASSEMBLY	DESCRIPTION	ASSEMBLY	DESCRIPTION
7046684-00	1232, 1532, Ch. 7, 6 Level, Bi-Octal, Ref. File U-8164	7116226	1240, 1540, Ch. 1, Mod. 3, 200 FPI, Octal, Odd Parity, Ref. File U-7468

Address	Instruction	Address	Instruction
500	50-3400	500	50-3400
501	50-7310	501	50-7300
502	50-7201	502	36-0366
503	50-1307	503	12-0512
504	00-0534	504	45-0011
505	00-0534	505	73-0504
506	36-0000	506	50-1301
507	42-0003	507	00-0540
510	70-0002	510	00-0534
511	44-0004	511	50-2701
512	70-0000	512	50-3000
513	50-1107	513	50-1101
514	00-0002	514	00-0304
515	00-0002	515	00-0057
516	50-2107	516	50-2701
517	34-0516	517	50-4777
520	50-4606	520	50-2701
521	51-0002	521	50-2101
522	63-0525	522	34-0521
523	10-0003	523	32-0057
524	60-0513	524	12-0061
525	57-0004	525	16-0060
526	34-0513	526	17-0000
527	45-0536	527	56-0062
530	56-0533	530	34-0526
531	34-0507	531	63-0500
532	34-0540	532	55-0060
533	00-0147	533	60-0000
534	00-0151	534	60-0000
535	00-0000	535	40-0011
536	00-0000	536	16-4611
537	00-0000	537	16-4611

1219 BOOTSTRAPS (MAG TAPE)

ASSEMBLY	DESCRIPTION	ASSEMBLY	DESCRIPTION
7033107-00	1240, Ch. 7, Mod 6, (Dual Channel), 556 FPI, Bi-Octal, Odd Parity, Ref. File U-7284A	7046678-00	1240, 1540, 1541, Ch. 7, Mod. 6 (Dual Channel), 556 FPI, Octal, Odd Parity, Ref. File U-7468

Address	Instruction	Address	Instruction
500	50-3400	500	50-3400
501	50-7310	501	50-7300
502	36-0366	502	36-0366
503	12-0537	503	12-0512
504	45-0011	504	45-0011
505	73-0504	505	73-0504
506	50-1307	506	50-1307
507	00-0544	507	00-0540
510	00-0534	510	00-0533
511	50-2707	511	50-2707
512	57-0057	512	50-3000
513	50-4777	513	50-1107
514	50-2707	514	00-0304
515	50-1107	515	00-0073
516	00-0310	516	50-2707
517	00-0076	517	50-4777
520	57-0057	520	50-2707
521	50-4777	521	50-2107
522	50-2707	522	34-0521
523	50-2107	523	32-0073
524	34-0523	524	12-0075
525	32-0076	525	16-0074
526	37-7776	526	17-0000
527	13-0000	527	56-0076
530	44-0200	530	34-0526
531	50-3000	531	63-0500
532	50-2407	532	55-0074
533	55-0200	533	60-0000
534	20-0000	534	60-0000
535	40-0011	535	40-0011
536	16-3300	536	16-3711
537	50-3000	537	16-3711

1219 BOOTSTRAP

(MAG TAPE)		(CARD PROCESSOR)	
ASSEMBLY	DESCRIPTION	ASSEMBLY	DESCRIPTION
7116236	1240/1540, Channel 3, Mod 3, Single, 556 F.P.I. Bioctal Odd Parity, Ref. File U-7468	7033157-00	1004 Card Processor/ with Standard Test Board (4010507-00), Single Channel, Channel 11, Ref. File U-8145.

Address	Instruction	Address	Instruction
00500	50-3400	500	50-3400
00501	50-7300	501	50-7300
00502	36-0366	502	50-7200
00503	12-0512	503	40-0451
00504	45-0011	504	50-1211
00505	73-0504	505	00-0550
00506	50 1303	506	00-0537
00507	00-0540	507	50-1111
00510	00-0534	510	00-0447
00511	50-2703	511	00-0400
00512	50-3000	512	50-2111
00513	50-1103	513	34-0512
00514	00-0304	514	12-0451
00515	00-0063	515	63-0524
00516	50-2703	516	32-0412
00517	50-4777	517	12-0413
00520	50-2703	520	44-0451
00521	50-2103	521	12-0414
00522	34-0521	522	44-0452
00523	32-0063	523	34-0504
00524	12-0065	524	50-7201
00525	16-0064	525	36-0031
00526	17-0000	526	11-0412
00527	56-0066	527	50-7200
00530	34-0526	530	47-0000
00531	63-0500	531	56-0451
00532	55-0064	532	34-0534
00533	60-0000	533	55-0452
00534	60-0000	534	50-7201
00535	40-0011	535	73-0526
00536	16-4211	536	34-0504
00537	16-4211	537	74-6000

1219 BOOTSTRAPS (MAG TAPE)

ASSEMBLY	DESCRIPTION	ASSEMBLY	DESCRIPTION
7046680-00	1240, 1540, 1541, Ch. 13, Mod. 3, 556 FPI, Octal, Odd Parity, Ref. File U-7468	7046680-00	1240, 1540, 1541, Ch. 7, Mod. 3, 556 FPI, Octal, Odd Parity, Ref. File U-

Address	Instruction	Address	Instruction
500	50-3400	500	50-3400
501	50-7300	501	50-7300
502	36-0366	502	36-0366
503	12-0512	503	12-0512
504	45-0011	504	45-0011
505	73-0504	505	73-0504
506	50-1313	506	50-1307
507	00-0540	507	00-0540
510	00-0534	510	00-0534
511	50-2713	511	50-2707
512	50-3000	512	50-3000
513	50-1113	513	50-1107
514	00-0304	514	00-0304
515	00-0263	515	00-0073
516	50-2713	516	50-2707
517	50-4777	517	50-4777
520	50-2713	520	50-2707
521	50-2113	521	50-2107
522	34-0521	522	34-0521
523	32-0263	523	32-0073
524	12-0265	524	12-0075
525	16-0264	525	16-0074
526	17-0000	526	17-0000
527	56-0266	527	56-0076
530	34-0526	530	34-0526
531	63-0500	531	63-0500
532	55-0264	532	55-0074
533	60-0000	533	60-0000
534	60-0000	534	60-0000
535	40-0011	535	40-0011
536	16-4711	536	16-4711
537	16-4711	537	16-4711

1219 BOOTSTRAP (MAG TAPE)

ASSEMBLY	DESCRIPTION	ASSEMBLY	DESCRIPTION
7116231	1240/1540, Chan 7, Mod 3, Single, 556 F.P.I., Octal Odd parity, Ref. File U-7468	7116235	1240/1540, Chan 7, Mod 3, Single, 556 F.P.I., Bioctal Odd parity, Ref. File U-7468

Address	Instruction	Address	Instruction
00500	50-3400	00500	50-3400
00501	50-7300	00501	50-7300
00502	36-0366	00502	36-0366
00503	12-0512	00503	12-0512
00504	45-0011	00504	45-0011
00505	73-0504	00505	73-0504
00506	50-1307	00506	50-1307
00507	00-0540	00507	00-0540
00510	00-0534	00510	00-0534
00511	50-2707	00511	50-2707
00512	50-3000	00512	50-3000
00513	50-1107	00513	50-1107
00514	00-0304	00514	00-0304
00515	00-0073	00515	00-0073
00516	50-2707	00516	50-2707
00517	50-4777	00517	50-4777
00520	50-2707	00520	50-2707
00521	50-2107	00521	50-2107
00522	34-0521	00522	34-0521
00523	32-0073	00523	32-0073
00524	12-0075	00524	12-0075
00525	16-0074	00525	16-0074
00526	17-0000	00526	17-0000
00527	56-0076	00527	56-0076
00530	34-0526	00530	34-0526
00531	63-0500	00531	63-0500
00532	55-0074	00532	55-0074
00533	60-0000	00533	60-0000
00534	60-0000	00534	60-0000
00535	40-0011	00535	40-0011
00536	16-4711	00536	16-4211
00537	16-4711	00537	16-4211